

## Low Capacitance TVS Diode Array

### Features

- ◆ 150 Watts Peak Power per Line ( $t_p = 8/20\mu s$ )
- ◆ Protects two I/O lines
- ◆ Low operating voltage: 5V
- ◆ Ultra Low capacitance ( $< 1.0pF$ ) for high-speed interfaces
- ◆ Solid-state technology

### IEC COMPATIBILITY (EN61000-4)

- ◆ IEC 61000-4-2 (ESD)  $\pm 15kV$  (air),  $\pm 8kV$  (contact)
- ◆ IEC 61000-4-4 (EFT) 40A (5/50ns)
- ◆ IEC 61000-4-5 (Lightning) 6A (8/20 $\mu s$ )

### Mechanical Characteristics

- ◆ JEDEC SOT-143 package
- ◆ Molding compound flammability rating: UL 94V-0
- ◆ Marking : Making Code
- ◆ Packaging : Tape and Reel per EIA 481
- ◆ RoHS/WEEE Compliant

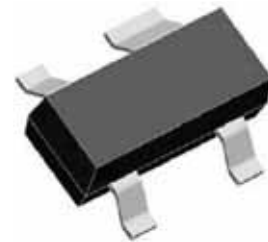
### Applications

- ◆ 10/100 Ethernet
- ◆ FireWire & USB
- ◆ Sensitive Analog Inputs
- ◆ Portable Electronics
- ◆ LAN/WAN equipment
- ◆ Video Line Protection
- ◆ Microcontroller Input Protection

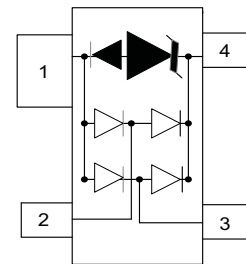
### Absolute Maximum Rating

Rating	Symbol	Value	Units
Peak Pulse Power ( $t_p = 8/20\mu s$ )	PPP	150	Watts
Peak Pulse Current ( $t_p = 8/20\mu s$ )	IPP	6	A
Lead Soldering Temperature	T <sub>L</sub>	260(10sec)	°C
Operating Temperature	T <sub>J</sub>	-55 to +125	°C
Storage Temperature	T <sub>STG</sub>	-55 to +150	°C

**SOT-143**

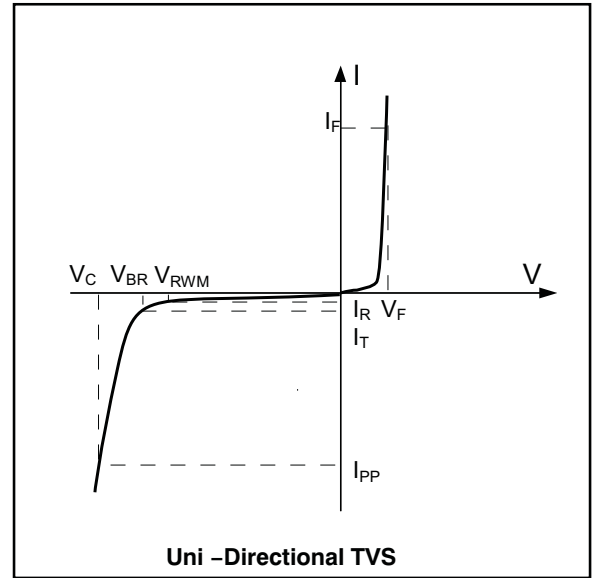


**PIN CONFIGURATION**



**ELECTRICAL CHARACTERISTICS**  
(TA = 25°C unless otherwise noted)

Symbol	Parameter
$V_{RWM}$	Peak Reverse Working Voltage
$I_R$	Reverse Leakage Current @ $V_{RWM}$
$V_{BR}$	Breakdown Voltage @ $I_T$
$I_T$	Test Current
$I_{PP}$	Maximum Reverse Peak Pulse Current
$V_C$	Clamping Voltage @ $I_{PP}$
$P_{PP}$	Peak Pulse Power
$C_J$	Junction Capacitance
$I_F$	Forward Current
$V_F$	Forward Voltage @ $I_F$



**Electrical Characteristics**

Parameter	Symbol	Conditions	Minimum	Typical	Maximum	Units
Reverse Stand-Off Voltage	$V_{RWM}$				5.0	V
Breakdown Voltage	$V_{BR}$	$I_T=1\text{mA}$	6.0			V
Reverse Leakage Current	$I_R$	$V_{RWM}=5\text{V}, T=25^\circ\text{C}$			1.0	$\mu\text{A}$
Clamping Voltage	$V_C$	$I_{PP}=1\text{A}, t_p=8/20\mu\text{s}$		10		V
Clamping Voltage	$V_C$	$I_{PP}=6\text{A}, t_p=8/20\mu\text{s}$		25		V
Junction Capacitance	$C_j$	Between I/O pins and Ground $V_R=0\text{V}, f=1\text{MHz}$		0.8	1.0	pF
		Between I/O pins $V_R=0\text{V}, f=1\text{MHz}$		0.4	0.6	pF

# RATING AND CHARACTERISTICS CURVES (TEP5VS143LC)

Figure 1: Peak Pulse Power Vs Pulse Time

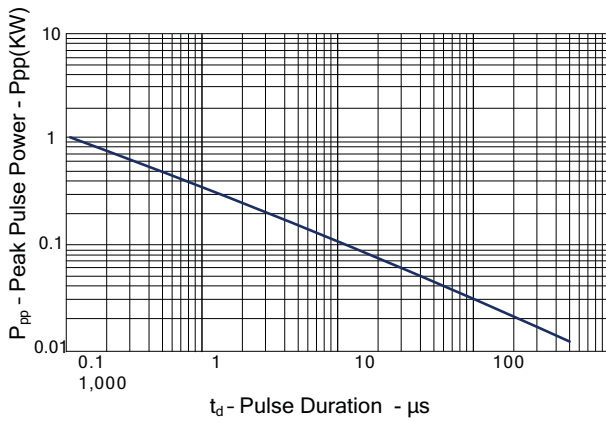


Figure 2: Power Derating Curve

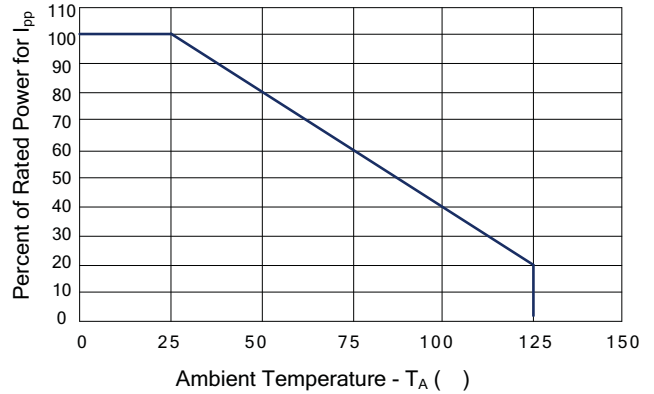


Figure 3: Pulse Waveform

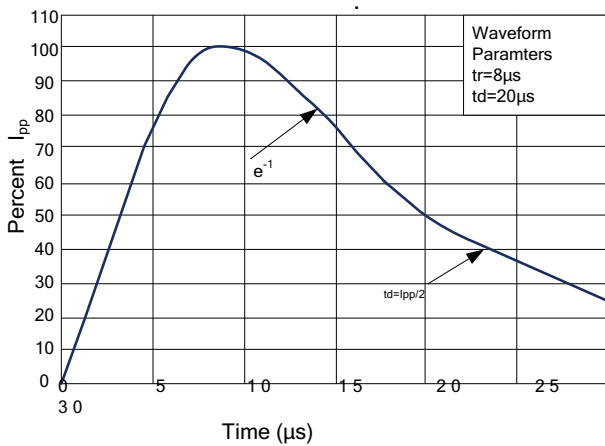


Figure 4: Clamping Voltage vs. Peak Pulse Current

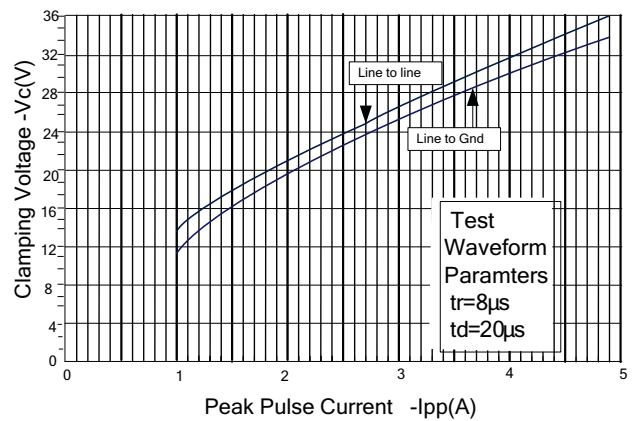


Figure 5: Forward Voltage vs. Forward Current

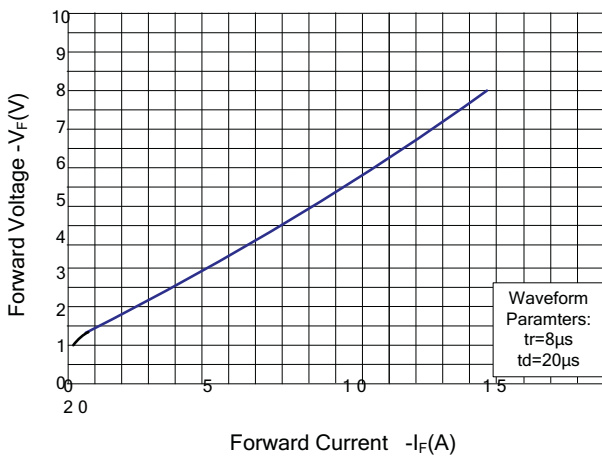
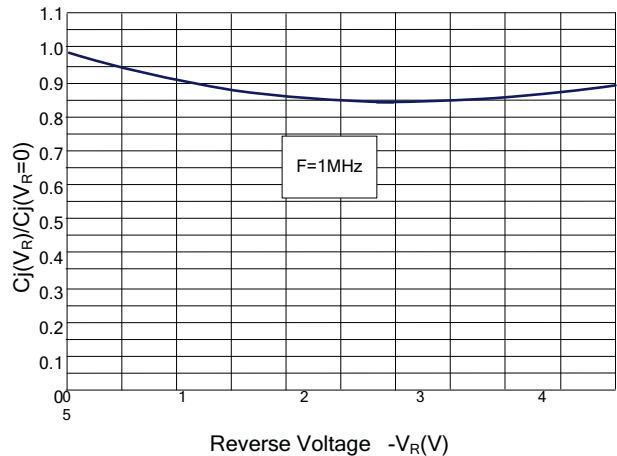


Figure 6: Capacitance vs. Reverse Voltage



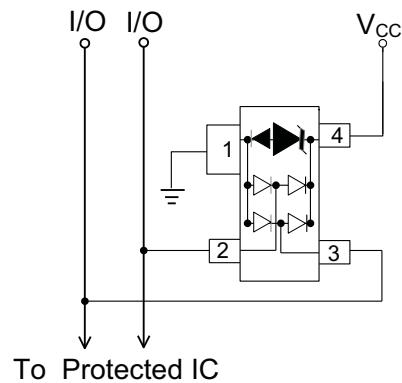
## Application Information

### Device Connection Options for Protection of Two High-Speed Data Lines

The TVS is designed to protect two data lines from transient over-voltages by clamping them to a fixed reference. When the voltage on the protected line exceeds the reference voltage (plus diode  $V_F$ ) the steering diodes are forward biased, conducting the transient current away from the sensitive circuitry. Data lines are at pins 2 and 3. The negative reference (REF1) is connected at pin 1. This pin should be connected directly to a ground plane on the board for the best results. The path length is kept as short as possible to minimize parasitic inductance. The reference (REF2) is connected at pin 4. The options for connecting the positive reference are as follows:

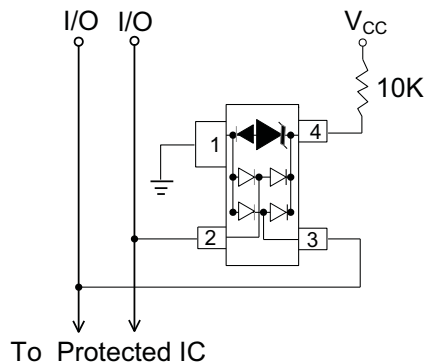
#### Data Line and Power Supply Protection Using $V_{CC}$ as reference

1. To protect data lines and the power line, connect pin 4 directly to the positive supply rail ( $V_{CC}$ ). In this configuration the data lines are referenced to the supply voltage. The internal TVS diode prevents over-voltage to the supply rail.



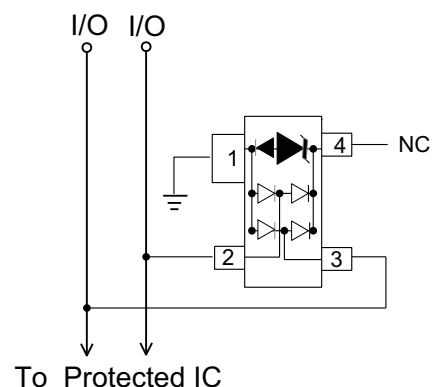
#### Data Line Protection with Bias and Power Supply Isolation Resistor

2. The  $V_{CC}$  can be isolated from the power supply by adding a series resistor between pin 4 and  $V_{CC}$ . A value of  $10k\Omega$  is recommended. The internal TVS and steering diodes remains biased, providing the advantage of lower capacitance.



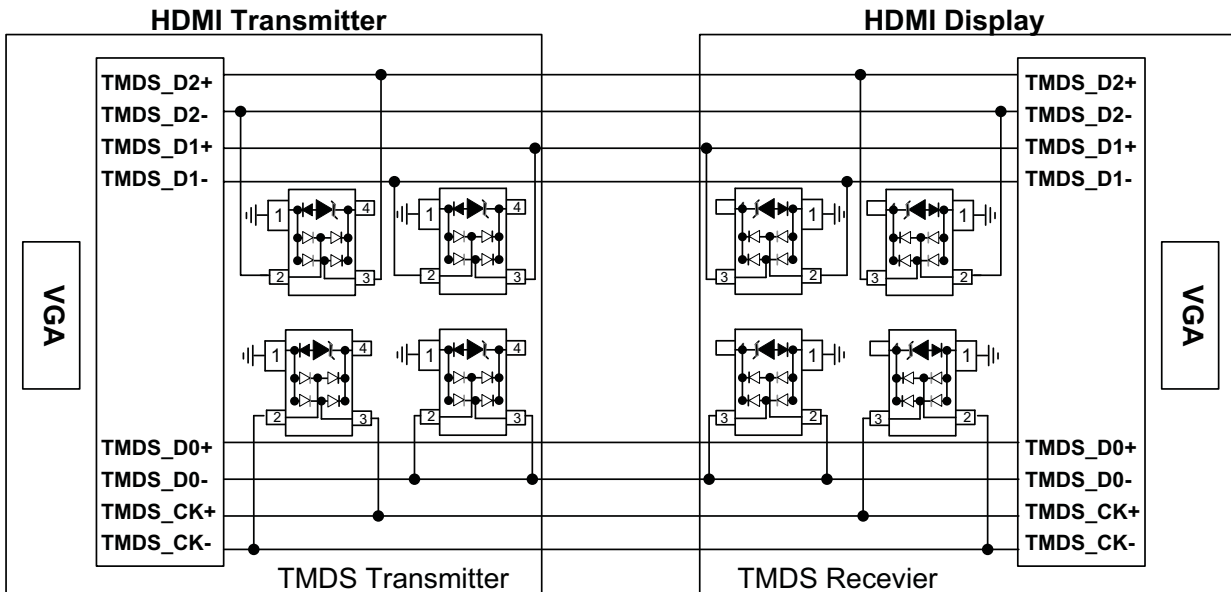
#### Data Line Protection Using Internal TVS Diode as Reference

3. In applications where no positive supply reference is available, or complete supply isolation is desired, the internal TVS may be used as the reference. In this case, pin 4 is not connected. The steering diodes will begin to conduct when the voltage on the protected line exceeds the working voltage of the TVS (plus one diode drop).



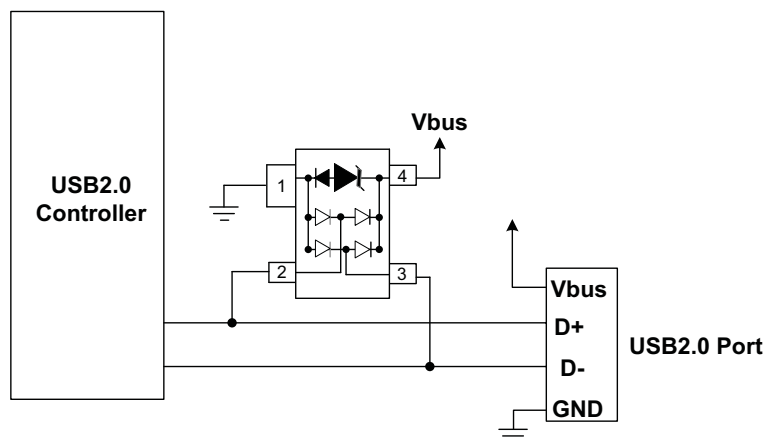
## Typical Applications

### HDMI Port Application



HDMI ports have become standard features on today's consumer electronics devices, such as digital TVs, DVD recorders, and set top boxes. The small geometry of a HDMI graphic chip will make it more susceptible to ESD and cable discharge events. The high-speed transmission requires the protection device to have low capacitance to maintain signal integrity and low clamping voltage to reduce stress on the IC. The offers full protection against ESD and its low capacitance of 0.6pF, ensures signal integrity.

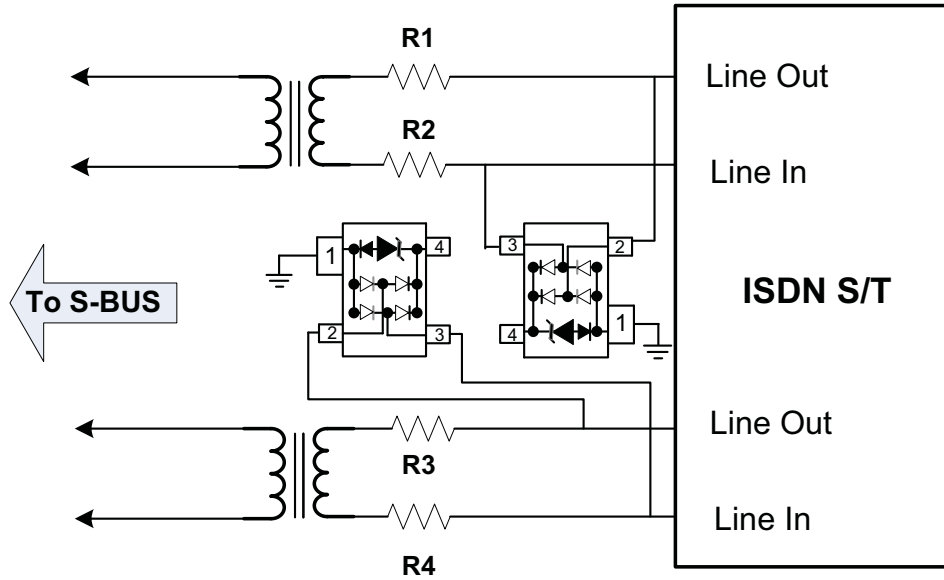
### USB2.0 Port Application



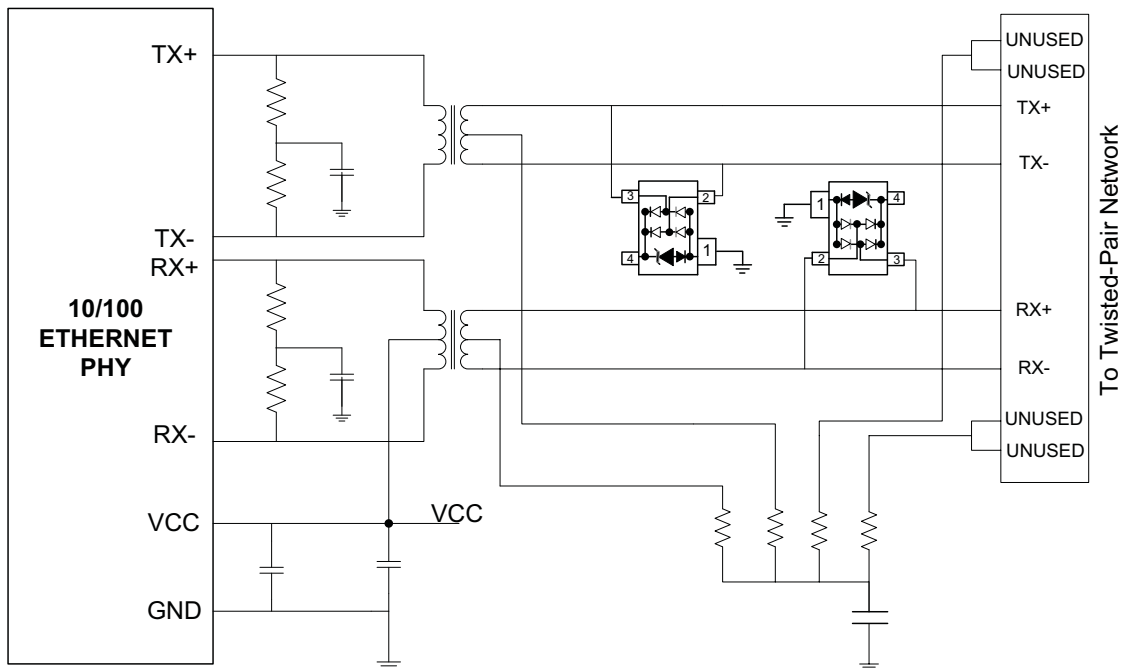
The can also be used to protect USB2.0 ports on monitors, computers, peripherals or portable systems.

Each device is able to protect single USB2.0 port. When the voltage on the data lines exceed the bus voltage (plus one diode drop), the internal diodes are forward biased conducting the transient current away from the protected controller chip. The TVS diode directs the surge to ground. The TVS diode also acts to suppress ESD strikes directly on the voltage bus. Thus, both power and data lines are protected.

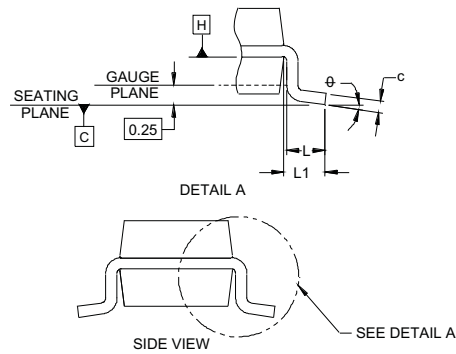
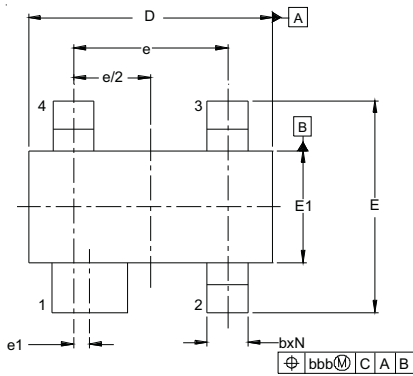
### ISDN S/T Interface Application



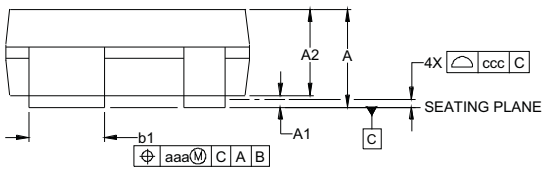
### 10/100 Ethernet Application



## Outline Drawing - SOT-143



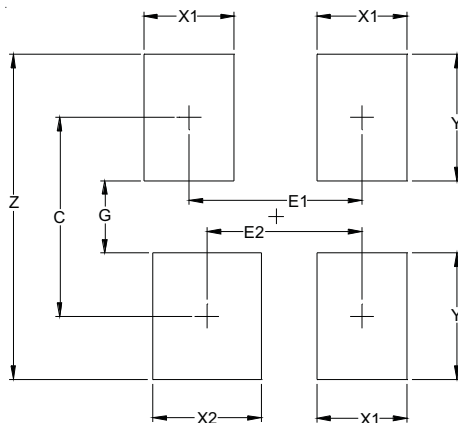
DIM	INCHES		MILLIMETERS	
	MIN	NOM/MAX	MIN	NOM/MAX
A	.031	-.048	0.80	- 1.22
A1	.000	-.006	0.013	- 0.15
A2	.029	.035	.042	0.75 0.90 1.07
b	.011	-.020	0.30	- 0.51
b1	.029	-.037	0.76	- 0.94
c	.003	-.008	0.08	- 0.20
D	.110	.114	.120	2.80 2.90 3.04
E	.082	.093	.104	2.10 2.37 2.64
E1	.047	.051	.055	1.20 1.30 1.40
e	.075 1.92 BSC			
e1	.008 0.20 BSC			
L	.015	.020	.024	0.40 0.50 0.60
L1	(.021) (0.54)			
N	4			
φ	0°	- 8°	0°	- 8°
aaa	.006 0.15			
bbb	.008 0.20			
ccc	.004 0.10			



### NOTES:

1. CONTROLLING DIMENSIONS ARE IN MILLIMETERS (ANGLES IN DEGREES).
2. DATUMS **-A-** AND **-B-** TO BE DETERMINED AT DATUM PLANE **-H-**
3. DIMENSIONS "E1" AND "D" DO NOT INCLUDE MOLD FLASH, PROTRUSIONS OR GATE BURRS.
4. REFERENCE JEDEC STD TO-253, VARIATION D.

## Land Pattern - SOT-143



DIMENSIONS		
DIM	INCHES	MILLIMETERS
C	(.087)	(2.20)
E1	.076	1.92
E2	.068	1.72
G	.031	0.80
X1	.039	1.00
X2	.047	1.20
Y	.055	1.40
Z	.141	3.60

### NOTES:

1. THIS LAND PATTERN IS FOR REFERENCE PURPOSES ONLY CONSULT YOUR MANUFACTURING GROUP TO ENSURE YOUR COMPANY'S MANUFACTURING GUIDELINES ARE MET.
2. REFERENCE IPC-SM-782A.

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